Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 - 75 (Cancelled)

76. (CURRENTLY AMENDED) A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly [[in]] during self-test [[mode]], where N > 1, each clock domain having one or more capture ~~clock~~ clocks and one or more ~~a plurality of~~ scan cells, each capture clock comprising a ~~plurality~~ selected number of shift clock pulses and a selected number of capture clock ~~pulses;~~ pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said method comprising the steps of:

(a) generating and ~~shifting-in~~ loading N pseudorandum stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a ~~shift-in~~ shift operation;

(b) applying an ordered sequence of capture ~~clocks~~ clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture ~~clocks~~ clock pulses comprising at least two capture

clock pulses from two or more selected capture clocks, for controlling two or more clock domains, ~~placed~~ in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response; ~~and does not contain any said shift clock pulse during a capture operation;~~ and

(c) compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.

77. (Currently amended) The method of claim 76, wherein each said capture clock is programmable to contain ~~one or more~~ said selected number of shift clock pulses and said selected number of capture clock pulses for performing said ~~shift-in/compact~~ shift/compact and capture ~~operations~~ operation on all said scan cells within ~~one said~~ a selected clock domain controlled by said capture clock; wherein ~~said clock domain is solely controlled by said capture clock; and~~ all said shift clock pulses and said capture clock pulses in said capture clock ~~can be either~~ are selectively generated internally or

controlled externally, and can be selectively operated at their ~~operate either at its~~ rated clock speed (at-speed) or at a selected clock speed.

78. (Currently amended) The method of claim 76, further comprising providing N scan enable (SE) signals ~~each within one said clock~~ each controlling a selected clock domain; wherein all said [[SE]] scan enable (SE) signals are used to switch operations from ~~shift-in/compact~~ shift/compact to capture, and vice versa; and wherein each said scan enable (SE) signal is selectively ~~further said SE signals can be~~ generated internally or controlled externally, and [[are]] can be selectively operated ~~either at the~~ at its rated clock ~~speeds~~ speed or at a selected clock ~~speeds~~ speed.

79. (Currently amended) The method of claim 78, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive all said [[N]] scan enable (SE) signals so that [[all]] said [[GSE]] global scan enable (GSE) signal and all said [[SE]] scan enable (SE) signals can be operated at a selected reduced clock speed.

80. (New) The method of claim 76, wherein said generating and ~~shifting-in~~ loading N pseudorandom stimuli further comprises operating all said ~~N-capture clocks~~ shift clock pulses at selected clock speeds or at the same clock speed; wherein all said ~~N-capture~~

~~clocks~~ shift clock pulses are selectively skewed so that at any given time only ~~scan cells within~~ one or more said ~~clock domains~~ scan cells are changing states to reduce power consumption.

81. (Previously presented) The method of claim 76, further comprising the step of comparing said signatures with their expected signatures for error indication, after a predetermined limiting criterion is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assembly or shifting-out said signatures for comparison in an ATE (automatic test equipment).

82. (Currently amended) The method of claim 76, wherein said generating and ~~shifting-in~~ loading N pseudorandom stimuli further comprises using ~~a plurality of~~ one or more pseudorandom pattern generators (PRPGs) to generate said N pseudorandom stimuli.

83. (Previously presented) The method of claim 82, wherein said pseudorandom pattern generator (PRPG) further comprises using a phase shifter connected to said PRPG outputs to generate one or more said pseudorandom stimuli.

84. (Previously presented) The method of claim 83, wherein said phase shifter is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

85. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises applying ~~two or more~~ said capture ~~clocks~~ clock pulses concurrently to two or more selected [[on]] clock domains which do not interact with each other or do not have any logic block crossing each other, for detecting or locating said faults in said selected clock domains ~~controlled by said capture clocks~~.

86. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises applying a reversed ordered sequence of capture ~~clocks~~ clock pulses from said ordered sequence of capture ~~clocks~~ clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

87. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively applying a shortened or expanded ordered sequence of capture ~~clocks~~ clock pulses from said ordered sequence of capture ~~clocks~~ clock pulses, for detecting or locating additional faults in said integrated circuit or circuit assembly.

88. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises disabling all capture clock pulses in one or more capture clocks, to facilitate fault diagnosis.

89. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at a selected clock speed, for detecting or locating stuck-at faults within [[the]] said selected clock domain ~~controlled by said capture clock~~.

90. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at [[its]] their rated clock speed, for detecting or locating delay faults within [[the]] said selected clock domain ~~controlled by said capture clock~~.

91. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively reducing the speed of all said capture clock ~~speed~~ pulses controlling a selected clock domain to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within [[the]] said selected clock domain ~~controlled~~

~~by said capture clock are tested~~ are detected or located at a predetermined rated clock speed.

92. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively operating [[two]] all said capture ~~clocks~~ clock pulses controlling two selected clock domains at selected clock speeds, for detecting or locating stuck-at faults crossing [[two]] said two selected clock domains.

93. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively adjusting the relative clock delay of two said capture ~~clocks operating at~~ clock pulses controlling two selected clock ~~speeds~~ domains, for detecting or locating delay faults crossing [[two]] said two selected clock domains.

94. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises selectively adjusting the relative clock delay of two said capture ~~clocks~~ clock pulses controlling two selected clock domains to the level, where delay faults associated with all multiple-cycle paths of equal cycle latency crossing [[two]] said two selected clock domains are ~~tested~~ detected or located at a predetermined rated clock speed.

95. (Currently amended) The method of claim 76, wherein said applying an ordered sequence of capture ~~clocks~~ clock pulses further comprises controlling the relative clock delay between any two adjacent capture ~~clocks internally~~ clock pulses inside or external to said integrated circuit or circuit assembly.

96. (Currently amended) The method of claim 76, wherein said compacting N output responses further comprises using ~~a plurality of~~ one or more multiple-input signature registers (MISRs) to generate said signatures.

97. (Previously presented) The method of claim 96, wherein said multiple-input signature register (MISR) further comprises using a space compactor connected to said MISR inputs for compressing said output responses to generate one or more said signatures.

98. (Previously presented) The method of claim 97, wherein said space compactor is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

99. (Currently amended) The method of claim 76, further comprising using a PRPG-MISR (pseudorandom pattern generator and multiple-input signature register) pair to detect or locate said faults within ~~a plurality of~~ one or more selected clock domains when [[the]] all said capture clocks controlling said ~~plurality of~~

selected clock domains operate at the same clock speed; wherein all said capture clocks are selectively skewed so as to eliminate races and timing violation during said ~~shift-in~~ shift, said capture, or said compact operation.

100. (Previously presented) The method of claim 99, wherein said PRPG-MISR pair further comprises a PRPG, selectively a phase shifter, selectively a space compactor, a MISR, and selectively a comparator.

101. (Canceled)

102. (Previously presented) The method of claim 76, wherein said compacting N output responses further comprises selectively comparing said N output responses directly with their expected output responses and indicating errors immediately using a compare operation.

103. (Previously presented) The method of claim 76, wherein said scan cell is selectively a multiplexed D flip-flop or a level-sensitive scan latch, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

104. (Previously presented) The method of claim 76, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprise other stuck-type faults, such as open faults and bridging faults, and wherein said delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay) faults, multiple-cycle delay faults, and path-delay faults.

105. (Currently amended) An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly [[in]] during self-test [[mode]], where N > 1, each clock domain having one or more capture [[clock]] clocks and ~~a plurality of~~ one or more scan cells, each capture clock comprising a ~~plurality~~ selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said apparatus comprising:

(a) means for generating and ~~shifting-in~~ loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a ~~shift-in~~ shift operation;

(b) means for applying an ordered sequence of capture ~~clocks~~ clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture ~~clocks~~ clock pulses comprising at least two said capture clock pulses from two or more selected capture clocks for controlling two or more clock domains, ~~placed~~ in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response ~~and does not contain any said shift clock pulse, during a capture operation~~; and

(c) means for compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.

106. (Currently amended) The apparatus of claim 105, wherein each said means of (a)-(c) [[are]] is selectively placed inside or external to said integrated circuit or circuit assembly.

Claims 107 - 134 (Canceled)